MIL-S-19500/189B
18 January 1972
SUPERSEDING
MIL-S-19500/189A
26 April 1966

MILITARY SPECIFICATION

SEMICONDUCTOR DEVICE, TRANSISTOR, PNP, GERMANIUM, LOW-POWER
TYPES 2N1224 AND 2N1225

This specification is mandatory for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for a PNP, germanium, high-frequency, low-power transistor.

1.2 Physical dimensions. See figure 1 (TO-33).

* 1.3 Maximum ratings.

P_T 1/ T_A = 25°C	P_T 2/ T_C = 25°C	V_{EBO}	V_{CBO}	I_C	T_{stg} & T_{op}
mW	mW	Vdc	Vdc	mAdc	°C
120	240	-0.5	-40	-10	-55 to +100

1/ Derate linearly 1.6 mW/°C for $T_A > 25$°C.
2/ Derate linearly 3.2 mW/°C for $T_C > 25$°C.

* 1.4 Primary electrical characteristics.

Limits	G_{pe} V_{CE} = -9 Vdc I_E = 1 mAdc f = 12.5 MHz	G_{pb} V_{CB} = -12 Vdc I_E = 1.5 mAdc f = 50 MHz	$\|h_{fe}\|$ V_{CE} = -12 Vdc I_C = -1.5 mAdc f = 10 MHz		C_{obo} V_{CB} = -12 Vdc I_E = 0 100 kHz ≤ f ≤ 1 MHz
	2N1224	2N1225	2N1224	2N1225	
	dB	dB			pF
Min	17	13	3	5	---
Max	27	21	16	16	3

2. APPLICABLE DOCUMENTS

2.1 The following documents, of the issue in effect on date of invitation for bids or request for proposal, form a part of the specification to the extent specified herein.

SPECIFICATION

MILITARY

MIL-S-19500 - Semiconductor Devices, General Specification for.

STANDARDS

MILITARY

* MIL-STD-202 - Test Methods for Electronic and Electrical Component Parts.
MIL-STD-750 - Test Methods for Semiconductor Devices.

(Copies of specifications, standards, drawings, and publications required by suppliers in connection with specific procurement functions should be obtained from the procuring activity or as directed by the contracting officer.)

3. REQUIREMENTS

3.1 General. Requirements shall be in accordance with MIL-S-19500, and as specified herein.

3.2 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-S-19500.

3.3 Design, construction, and physical dimensions. Transistors shall be of the design, construction, and physical dimensions shown on figure 1.

* 3.3.1 Lead material and finish. Lead material shall be Kovar or alloy 52. Lead finish shall be gold-plated. (Leads may be tin-coated if specified in the contract or order, and this requirement shall not be construed as adversely affecting the qualified-product status of the device, or applicable JAN marking (see 6.2)).

* 3.3.1.1 Selectivity of lead material. Where choice of lead material (see 3.3.1 above) is desired, it shall be specified in the contract or order (see 6.2).

3.4 Performance characteristics. Performance characteristics shall be as specified in tables I, II, and III.

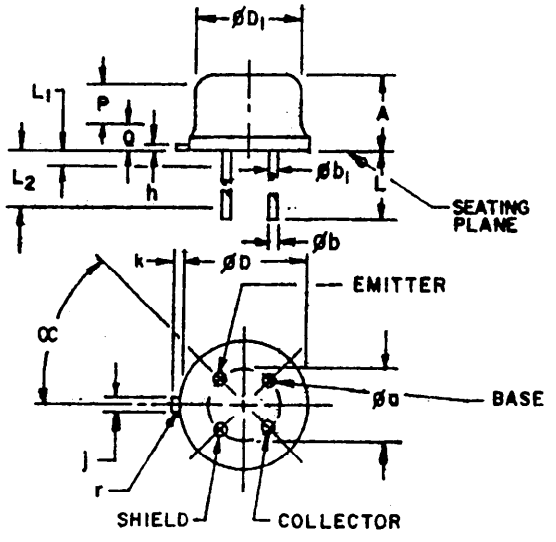
3.5 Marking. The following marking specified in MIL-S-19500 may be omitted from the body of the transistor at the option of the manufacturer:

(a) Country of origin.
(b) Manufacturer's identification.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection shall be in accordance with MIL-S-19500, and as specified herein.

4.2 Qualification inspection. Qualification inspection shall consist of the examinations and tests specified in tables I, II, and III.

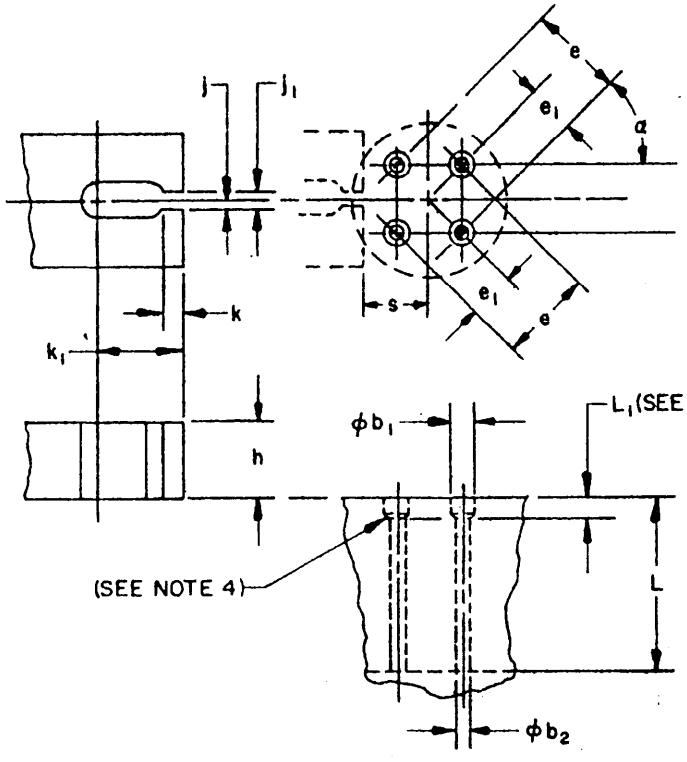


LTR	DIMENSIONS				NOTES
	INCHES		MILLIMETERS		
	MIN	MAX	MIN	MAX	
A	.240	.260	6.10	6.60	
Øa	.200 TP		5.08 TP		6
Øb	.016	.021	.41	.53	7, 8
$Øb_1$	.016	.019	.41	.48	7, 8
ØD	.335	.370	8.51	9.40	
$ØD_1$	.305	.335	7.75	8.51	
h	.009	.041	.23	1.04	
j	.028	.034	.71	.86	2
k	.029	.045	.74	1.14	3
L	1.500	1.750	38.10	44.45	7, 8
L_1	---	.050	---	1.27	7, 8
L_2	.250	---	6.35	---	7, 8
P	.100	---	2.54	---	5
Q	---	.050	---	1.27	4
r	---	.010	---	.25	10
α	45° TP		45° TP		6

NOTES:
1. Metric equivalents (to the nearest .01 mm) are given for general information only and are based upon 1 inch = 25.4 mm.
2. Beyond r(radius) maximum, j shall be held for a minimum length of .011(.28 mm).
3. k measured from maximum ØD.
4. Outline in this zone is not controlled.
5. $ØD_1$ shall not vary more than .010(.25 mm) in zone P. This zone is controlled for automatic handling.
6. Leads at gage plane .054 + .001-.000(1.37 + .03-.00 mm) below seating plane shall be within .007(.18 mm) radius of True Position (TP) at maximum material condition (MMC) relative to tab at MMC. The device may be measured by direct methods or by the gage and gaging procedure shown in Figure 2.
7. $Øb_1$ applies between L_1 and L_2. Øb applies between L_2 and L minimum. Diameter is uncontrolled in L_1 and beyond L minimum.
8. All four leads.
9. The shield lead shall be internally connected to the case. The other three leads shall be electrically insulated from the case.
10. r(radius) applies to both inside corners of tab.

FIGURE 1. Physical dimensions of transistor types 2N1224 and 2N1225 (TO-33).

LTR	DIMENSIONS				NOTES
	INCHES		MILLIMETERS		
	MIN	MAX	MIN	MAX	
ϕb_1	.0595	.0605	1.51	1.54	
ϕb_2	.0325	.0335	.83	.85	
e	.1995	.2005	5.07	5.09	
e_1	.0995	.1005	2.53	2.55	
h	.150 Nominal		3.81 Nominal		
j	.0175	.0180	.44	.46	
j_1	.0350	.0355	.89	.90	
k	.009	.011	.23	.28	
k_1	.125 Nominal		3.18 Nominal		
L	.372	.378	9.45	9.60	
L_1	.054	.055	1.37	1.40	
S	.182	.199	4.62	5.05	1
α	44.90°	45.10°	44.90°	45.10°	



NOTES:
1. The location of the tab locator within the limits indicated will be determined by the tab and flange dimensions of the device being checked.
2. The following gaging procedure shall be used:

   The device being measured shall be inserted until its seating plane is .125(3.18 mm) ±.010(.25 mm) from the seating surface of the gage. A force of 8 ± .5 oz. shall then be applied parallel and symmetrical to the device's cylindrical axis. When examined visually after the force application (the force need not be removed) the seating plane of the device shall be seated against the gage.

   The use of a pin straightener prior to insertion in the gage is permissible.

3. Gaging plane.
4. Drill angle.

FIGURE 2. Gage for lead and tab location for transistor types 2N1224 and 2N1225.

Examination or test	MIL-STD-750		LTPD	Symbol	Limits		Unit
	Method	Details			Min	Max	
Subgroup 1			10				
Visual and mechanical examination	2071			---	---	---	---
Subgroup 2			5				
Collector to base cutoff current	3036	Bias condition D V_{CB} = -12 Vdc		I_{CBO}	---	-10	μAdc
Collector to emitter cutoff current	3041	Bias condition D V_{CE} = -20 Vdc		I_{CEO}	---	-1	mAdc
Small-signal short-circuit forward-current transfer ratio	3206	V_{CE} = -12 Vdc I_C = -1.5 mAdc		h_{fe}	30	175	---
Collector to base cutoff current	3036	Bias condition D V_{CB} = -40 Vdc		I_{CBO}	---	-20	μAdc
Emitter to base cutoff current	3061	Bias condition D V_{EB} = -0.5 Vdc		I_{EBO}	---	-6	μAdc
* Subgroup 3			10				
Noise figure	3246						
2N1224		V_{CE} = -9 Vdc; I_E = 1 mAdc f = 12.5 MHz; R_g = 150 ohms R_L = 2000 ohms		NF	---	10	dB
2N1225		V_{CB} = -12 Vdc; I_E = 1.5 mAdc f = 50 MHz; R_g = 30 ohms R_L = 2000 ohms		NF	---	10	dB
Small-signal power gain	3256						
2N1224		V_{CE} = -9 Vdc; I_E = 1 mAdc f = 12.5 MHz (see figure 3)		G_{pe}	17	27	dB
2N1225		V_{CB} = -12 Vdc; I_E = 1.5 mAdc f = 50 MHz (see figure 4)		G_{pb}	13	21	dB
Magnitude of common-emitter small-signal short-circuit forward-current transfer ratio	3306	V_{CE} = -12 Vdc; I_C = -1.5 mAdc f = 10 MHz					
2N1224				$\lvert h_{fe} \rvert$	3	16	---
2N1225				$\lvert h_{fe} \rvert$	5	16	---
Open-circuit output capacitance	3236	V_{CB} = -12 Vdc; I_E = 0 100 kHz $\leq$ f $\leq$ 1 MHz		C_{obo}	---	3	pF
* Subgroup 4			10				
High-temperature operation:		T_C = +85°C					
Collector to base cutoff current	3036	Bias condition D V_{CB} = -12 Vdc		I_{CBO}	---	-500	μAdc
Low-temperature operation:		T_C = -55°C					
Small-signal short-circuit forward-current transfer ratio	3206	V_{CE} = -12 Vdc I_C = -1.5 mAdc		h_{fe}	10	---	---

TABLE II. Group B inspection

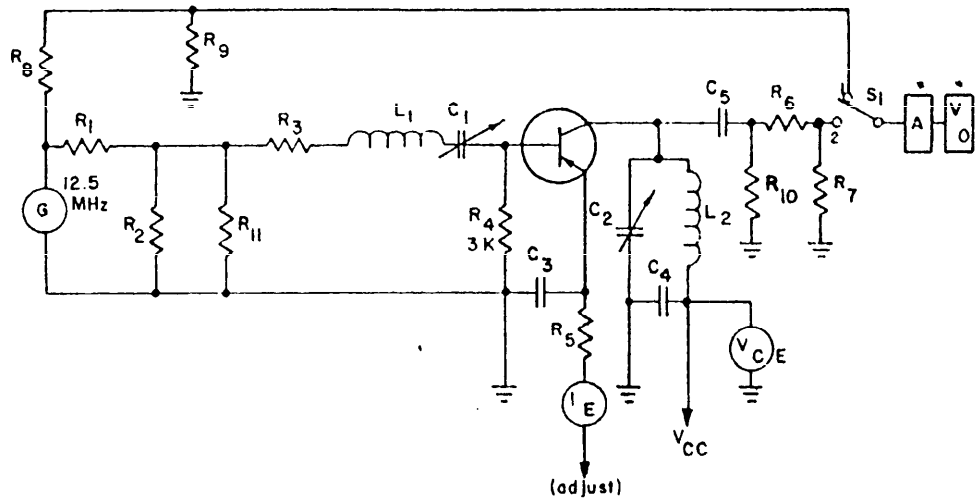
Examination or test	MIL-STD-750		LTPD	Symbol	Limits		Unit
	Method	Details			Min	Max	
Subgroup 1			20				
Physical dimensions	2066	(See figure 1)		---	---	---	---
* Subgroup 2			15				
Solderability	2026			---	---	---	---
Thermal shock (temperature cycling)	1051	Test condition B, except in step 3, T_A = +100 +5, -0°C		---	---	---	---
Thermal shock (glass strain)	1056	Test condition A		---	---	---	---
Hermetic seal	1071	Test condition G or H for fine leaks; test condition A, C, D, or F for gross leaks		---	---	$1x10^{-7}$	atm cc/s
Moisture resistance	1021			---	---	---	---
End points:							
Collector to base cutoff current	3036	Bias condition D V_{CB} = -40 Vdc		I_{CBO}	---	-20	μAdc
Small-signal short-circuit forward-current transfer ratio	3206	V_{CE} = -12 Vdc I_C = -1.5 mAdc		h_{fe}	30	175	---
* Subgroup 3			10				
Shock	2016	Nonoperating; 1500 G; 0.5 ms 5 blows in each orientation: X_1, Y_1, Y_2, and Z_1		---	---	---	---
Vibration, variable frequency	2056	10 G		---	---	---	---
Constant acceleration	2006	10,000 G; in each orientation: X_1, Y_1, Y_2, and Z_1		---	---	---	---
End points: (Same as subgroup 2)							
* Subgroup 4			20				
Terminal strength (lead fatigue)	2036	Test condition E		---	---	---	---
End points:							
Hermetic seal	1071	Test condition G or H for fine leaks; test condition A, C, D, or F for gross leaks		---	---	$1x10^{-7}$	atm cc/s
* Subgroup 5			20				
Salt atmosphere (corrosion)	1041			---	---	---	---

TABLE II. Group B inspection - continued

Examination or test	MIL-STD-750		LTPD	Symbol	Limits		Unit
	Method	Details			Min	Max	
* Subgroup 6			7				
High-temperature life (nonoperating)	1032	T_{stg} = +100°C (see 4.3.4)		---	---	---	---
End points:							
Collector to base cutoff current	3036	Bias condition D V_{CB} = -40 Vdc		I_{CBO}	---	-40	μAdc
Small-signal short-circuit forward-current transfer ratio	3206	V_{CE} = -12 Vdc I_C = -1.5 mAdc		h_{fe}	24	---	---
* Subgroup 7			7				
Steady-state operation life	1027	P_T = 120 mW; V_{CB} = -12 Vdc (see 4.3.4)		---	---	---	---
End points: (Same as subgroup 6)							

TABLE III. Group C inspection

Test	MIL-STD-750		LTPD	Symbol	Limits		Unit
	Method	Details			Min	Max	
Subgroup 1			20				
Thermal resistance	3151			θ_{J-A}	---	0.625	°C/mW
* Subgroup 2			10				
Resistance to solvents	---	MIL-STD-202, Method 215 (see 4.4.2)		---	---	---	---
* Subgroup 3			λ=10				
High-temperature life (nonoperating)	1031	T_{stg} = +100°C (see 4.3.4)		---	---	---	---
End points: (Same as subgroup 6 of group B)							
* Subgroup 4			λ=10				
Steady-state operation life	1026	P_T = 120 mW; V_{CB} = -12 Vdc (see 4.3.4)		---	---	---	---
End points: (Same as subgroup 6 of group B)							

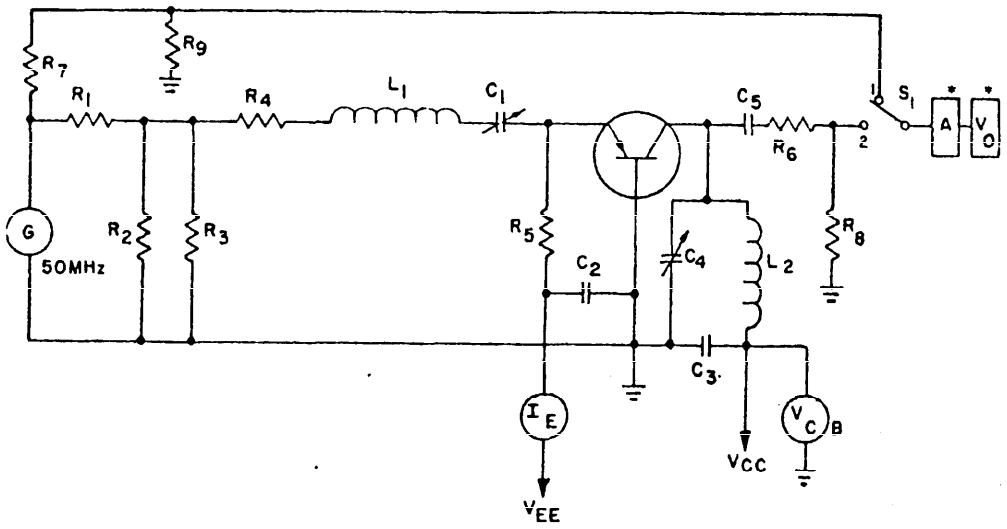


NOTE: *A = 12.5 MHz amplifier - 60 dB gain (voltage gain = 1000 times).
C_1, C_2 = 100 pF variable capacitor.
C_3, C_4, C_5 = 0.01 μF ceramic disc. capacitor.
G = 12.5 MHz oscillator, 50 ohms source impedance.
I_E = D.C. milliammeter ±2%.
L_1 = 3.5 μH.
L_2 = 3.5 μH.
R_1 = 45 ohms ± 1% (IRC Type MDB Resistor, or equivalent).
R_2, R_{11} = 10 ohms ±1% (IRC Type MDB Resistor, or equivalent).
R_3 = 150 ohms ±1% (IRC Type MDB Resistor, or equivalent).
R_4 = 3000 ohms 1/2 W carbon resistor.
R_5 = 1000 ohms.
R_6 = 275 ohms ±1% (IRC Type MDB Resistor, or equivalent).
R_7, R_9 = 50 ohms ±1% (IRC Type MDB Resistor, or equivalent).
R_8 = 2000 ohms ±1% (IRC Type MDB Resistor, or equivalent).
R_{10} = 150 ohms ±1% (IRC Type MDB Resistor, or equivalent).
S_1 = Thompson Con 3AA Coax Switch, or equivalent).
V_C = D.C. voltmeter ±2%.
*V_O = Hewlett Packard Model 410 VTVM, or equivalent.

*A suitable R_F voltmeter, such as Boonton Model 91CA, or equivalent, may be substituted for amplifier/voltmeter combination shown.

CALIBRATION: Set switch S_1 to position 1 and adjust signal to 0.5 volts on V_O meter. Set switch S_1 to position 2 and read V_O (minimum V_O = 300 millivolts for 17 dB power gain, P_g).

FIGURE 3. Power-gain test circuit for transistor type 2N1224.



NOTE: Case of transistor under test shall be grounded.
*A = 50 MHz amplifier - 60 dB gain (voltage gain = 1000 times).
C_1, C_4 = 50 pF variable capacitor.
C_2, C_3, C_5 = 0.01 μF ceramic disc. capacitor.
G = 50 MHz oscillator - 50 ohms source impedance.
I_E = D.C. milliammeter ±2%
L_1 = 0.196 μH (air core).
L_2 = 0.7 μH (air core).
R_1 = 45 ohms ±1% (IRC Type MDB Resistor, or equivalent).
R_2, R_3 = 10 ohms ±1% (IRC Type MDB Resistor, or equivalent).
R_4 = 25 ohms ±1% (IRC Type MDB Resistor, or equivalent).
R_5 = 3000 ohms, 2 W carbon resistor.
R_6 = 2000 ohms ±1% (IRC Type MDB Resistor, or equivalent).
R_7 = 750 ohms ±1% (IRC Type MDB Resistor, or equivalent).
R_8, R_9 = 50 ohms ±1 ,IRC Type MDB Resistor, or equivalent).
S_1 = Thompson Con 3AA Coax Switch, or equivalent.
V_C = D.C. voltmeter ±2%.
*V_O = Hewlett Packard Model 410B VTVM, or equivalent.

*A suitable R_F voltmeter, such as Boonton Model 91CA, or equivalent, may be substituted for amplifier/voltmeter combination shown.

CALIBRATION: Set switch S_1 to position 1 and adjust signal to 0.5 volts on V_O meter. Set switch S_1 to position 2 and read V_O (minimum V_O = 340 millivolts for 13 dB power gain, P_g).

FIGURE 4. Power-gain test circuit for transistor type 2N1225.

4.3 Quality conformance inspection. Quality conformance inspection shall consist of groups A, B, and C inspections.

4.3.1 Group A inspection. Group A inspection shall consist of the examinations and tests specified in table I.

4.3.2 Group B inspection. Group B inspection shall consist of the examinations and tests specified in table II.

4.3.3 Group C inspection. Group C inspection shall consist of the tests specified in table III. This inspection shall be conducted on the initial lot and thereafter every 6 months during production.

* 4.3.4 Group B and group C life-test samples. Samples that have been subjected to group B, 340-hour life-test, may be continued on test to 1, 000 hours in order to satisfy group C life-test requirements. These samples shall be predesignated, and shall remain subjected to the group C, 1, 000-hour acceptance evaluation after they have passed the group B, 340-hour acceptance criteria. The cumulative total of failures found during 340-hour test and during the subsequent interval up to 1, 000 hours shall be computed for 1, 000-hour acceptance criteria (see 4.3.3).

4.4 Methods of examination and test. Methods of examination and test shall be as specified in tables I, II, and III, and as follows:

4.4.1 Condition of the shield lead. The shield lead is open for the following tests: I_{CEO}, I_{CBO}, I_{EBO}, and C_{obo}. The shield lead is grounded for the following tests: h_{fe}, NF, G_{pb} and G_{pe}.

* 4.4.2 Resistance to solvents. Transistors shall be subjected to tests in accordance with method 215 of MIL-STD-202. The following details shall apply:

(a) All areas of the transistor body where marking has been applied shall be brushed.
(b) After subjection to the tests there shall be no evidence of mechanical damage to the device and markings shall have remained legible.

5. PREPARATION FOR DELIVERY

5.1 See MIL-S-19500, section 5.

6. NOTES

6.1 Notes. The notes specified in MIL-S-19500 are applicable to this specification.

* 6.2 Ordering data.

(a) Lead finish if other than gold-plated (see 3.3.1).
(b) Selectivity of lead material (see 3.3.1.1).

6.3 Changes from previous issue. The margins of this specification are marked with an asterisk to indicate where changes (additions, modification, corrections, deletions) from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

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Army - EL
Navy - EC
Air Force - 17

Review activities:
Army - MU, MI
Air Force - 11, 80
Navy - OS
DSA - ES

User activities:
Army - AV, SM
Navy - AS, CG, MC, SH
Air Force - 13, 15, 19

Preparing activity:
Army - EL

Agent:
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(Project 5961-0291)

STANDARDIZATION DOCUMENT IMPROVEMENT PROPOSAL

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